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TL7702B, TL7705B, TL7733B
ZHCSMQ2O – SEPTEMBER 1989 – REVISED DECEMBER 2020

TL7702B、TL7733B 和 TL7705B 电源电压监控器

1 特性

- 上电复位发生器
- 电压下降后自动复位生成
- $\overline{\text{RESET}}$ 输出定义为从 $V_{CC} \geqslant 1V$ 开始
- 精密电压传感器
- 温度补偿电压基准
- 真实和互补复位输出
- 外部可调脉冲持续时间

2 应用

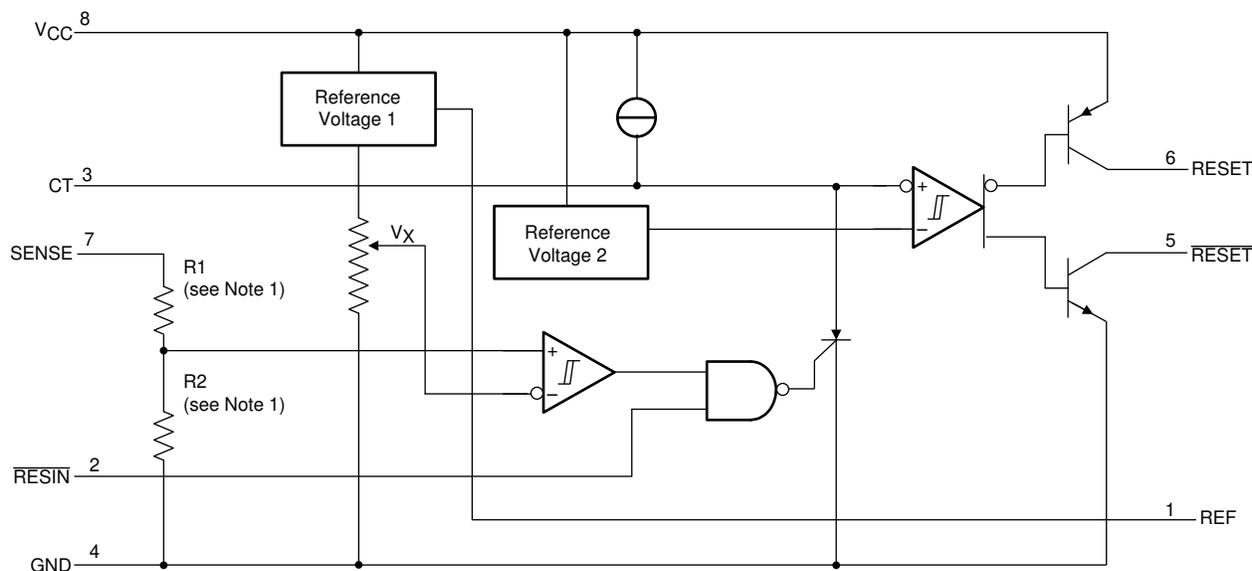- 无线通信系统
- 工厂自动化
- 楼宇自动化
- 服务器
- 笔记本电脑和台式机
- STB 和 DVR

3 说明

TL7702B、TL7705B 和 TL7733B 为集成电路电源电压监控器，旨在用作微型计算机和微处理器系统中的复位控制器。电源电压监控器监控 SENSE 输入端的电源是否欠压。正常运行期间，如果发生欠压，则输出 $\overline{\text{RESET}}$，且 RESET 激活。

TL7702BC、TL7705BC 和 TL7733BC 的工作温度范围为 0°C 至 +70°C。TL7702BI、TL7705BI 和 TL7733BI 的工作温度范围为 –40°C 至 +85°C。TL7705BQ 的工作温度范围为 –40°C 至 +125°C。

器件信息[1]

器件型号	封装	封装尺寸（标称值）
TL77xxBD	SOIC (8)	4.90mm × 3.91mm
TL77xxBP	PDIP (8)	9.81mm × 6.35mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

功能方框图

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English Data Sheet: SLVS037

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4 Revision History

Changes from Revision N (September 2016) to Revision O (December 2020)   **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式...1
- Corrected the $\overline{\text{RESIN}}$ pin description..3
- Corrected the I_{CC} parameter units from µA to mA in Electrical Characteristics Table.....................6

Changes from Revision M (May 2003) to Revision N (September 2016)   **Page**

- 添加了 *ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及 *机械、封装和可订购信息* 部分。...1
- 删除了 *订购信息* 表；请参阅数据表末尾的 POA...1
- Deleted Lead temperature row...4
- Changed R $_{\theta JA}$ for D (SOIC) from 97 to 109.2 and for P (PDIP) from 85 to 51.4...............................5

5 Pin Configuration and Functions
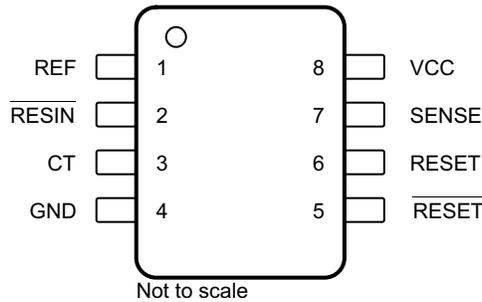
图 **5-1. D or P Package 8-Pin SOIC or PDIP Top View**

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CT	3	O	Timing capacitor input. The timing capacitor determines the time delay that the reset outputs remain active after the voltage at the SENSE input exceeds the positive-going threshold value.
GND	4	—	Ground
REF	1	O	Reference voltage. See 节 6.5 for reference voltage output and specification.
RESET	6	O	Active high reset. See 图 6-1 for RESET function and timing.
$\overline{\text{RESET}}$	5	O	Active low reset. See 图 6-1 for $\overline{\text{RESET}}$ function and timing.
$\overline{\text{RESIN}}$	2	I	Reset input. When the Reset Input is low, the RESET output goes high and the $\overline{\text{RESET}}$ goes low. When the Reset Input is high, the RESET and $\overline{\text{RESET}}$ outputs are allowed to trigger based on the SENSE voltage.
SENSE	7	I	Sense input. Voltage input to be supervised. See 图 6-1 for SENSE function and timing.
VCC	8	—	Supply voltage. See 节 6.3 for recommended voltage input range.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage[2], V_{CC}			20	V
Input voltage, V_I	$\overline{RESIN}$	−0.3	20	V
	SENSE	−0.3	20	
High-level output current, I_{OH} (RESET)			−30	mA
Low-level output current, I_{OL} ($\overline{RESET}$)			30	mA
Operating virtual junction temperature, T_J			150	°C
Storage temperature, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3.6	18	V
V_{IH}	High-level input voltage	$\overline{RESIN}$	2	18	V
V_{IL}	Low-level input voltage	$\overline{RESIN}$	0	0.8	V
V_I	Input voltage	SENSE	0	18	V
I_{OH}	High-level output current	RESET		−20	mA
I_{OL}	Low-level output current	$\overline{RESET}$		20	mA
T_A	Operating free-air temperature	TL77xxBC	0	70	°C
		TL77xxBI	−40	85	
		TL7705BQ	−40	125	

6.4 Thermal Information

THERMAL METRIC[1] [2]		TL77xxB		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	109.2	51.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56	40.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.9	28.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.4	17.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	49.4	28.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

(2) Maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A) / R_{\theta JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

6.5 Electrical Characteristics: TL77xxBC, TL77xxBI, and TL7705BQ

over operating free-air temperature range (unless otherwise noted)[1]

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage, RESET		$I_{OH} = -16$ mA	$V_{CC} - 1.5$			V
V_{OL}	Low-level output voltage, $\overline{RESET}$		$I_{OL} = 16$ mA			0.4	V
V_{REF}	Reference voltage, REF		$I_{ref} = -500$ µA, $T_A = 25°C$	2.48	2.53	2.58	V
V_{IT-}	Negative-going input threshold voltage at SENSE input	TL7702B	$T_A = 25°C$	2.505	2.53	2.555	V
		TL7705B		4.5	4.55	4.6	
		TL7733B		3.03	3.08	3.13	
		TL7702B	$T_A = $ full range[2]	2.48	2.53	2.58	
		TL7705B		4.45	4.55	4.65	
		TL7733B		3	3.08	3.16	
V_{HYS}	Hysteresis, SENSE ($V_{IT+} - V_{IT-}$)	TL7702B	$V_{CC} = 3.6$ V to 18 V, $T_A = 25°C$		10		mV
		TL7705B			30		
		TL7733B			10		
V_{RES}	Power-up reset voltage[3]		I_{OL} at $\overline{RESET} = 2$ mA, $T_A = 25°C$			1	V
I_I	Input current	$\overline{RESIN}$	$V_I = 0.4$ V to V_{CC}			-10	µA
		SENSE, TL7702B	$V_I = V_{REF}$ to 18 V		-0.1	-2	
I_{OH}	High-level output current, $\overline{RESET}$		$V_O = 18$ V, see 图 7-1			50	µA
I_{OL}	Low-level output current, RESET		$V_O = 0$ V, see 图 7-1			-50	µA
I_{CC}	Supply current		$V_{SENSE} = 15$ V, $\overline{RESIN} \geqslant 2$ V		1.8	3	mA
			$V_{CC} = 18$ V, $T_A = $ full range[2]			3.5	

(1) All electrical characteristics are measured with 0.1-µF capacitors connected at REF, CT, and VCC to GND.
(2) Full range is 0°C to 70°C for the C-suffix devices, –40°C to 85°C for the I-suffix devices, and –40°C to 125°C for the Q-suffix device.
(3) This is the lowest voltage at which $\overline{RESET}$ becomes active.

6.6 Switching Characteristics: TL77xxBC, TL77xxBI, and TL7705BQ

$V_{CC} = 5$ V, C_T open, $T_A = 25°C$, over operating free-air temperature range (unless otherwise noted)

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time from low-level to high-level output	$\overline{RESIN}$	RESET	See , 图 6-1 图 6-2, 图 7-1		270	500	ns
t_{PHL}	Propagation delay time from high-level to low-level output	$\overline{RESIN}$	$\overline{RESET}$	See 图 6-1, 图 6-2, 图 7-2		270	500	ns
t_w	Effective pulse duration	$\overline{RESIN}$		See 图 7-3, 图 7-4		150		ns
		SENSE				100		
t_r	Rise time		RESET	See 图 6-1, 图 7-1, 图 7-2			75	ns
			$\overline{RESET}$			75	150	
t_f	Fall time		RESET	See 图 6-1, 图 7-1, 图 7-2		150	200	ns
			$\overline{RESET}$				50	

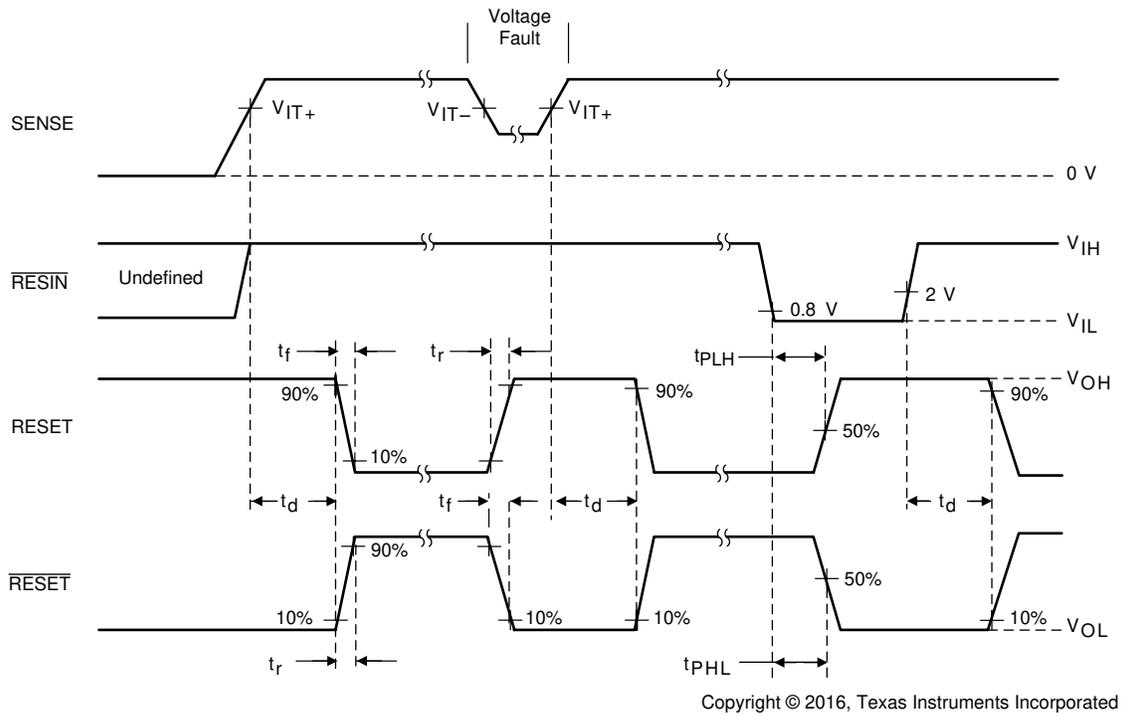## 6.7 Timing Diagrams

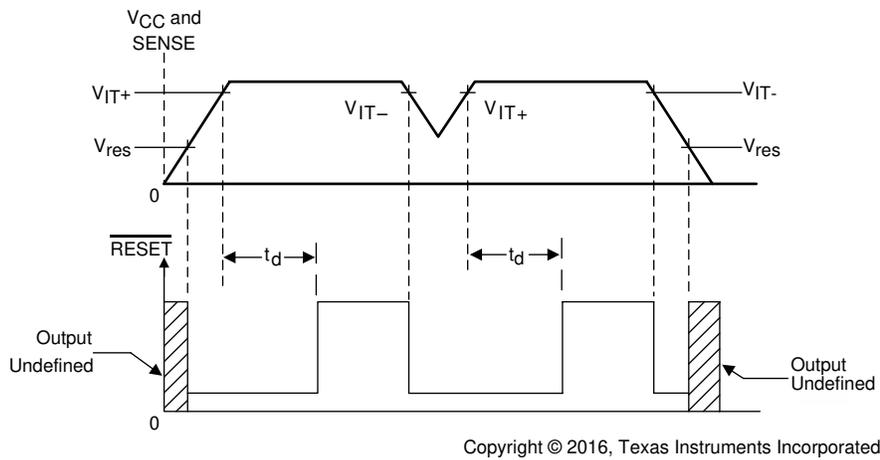图 **6-1. TL7702B, TL7705B, and TL7733B Timing Diagram**

图 **6-2. V$_{IT}$ and V$_{RES}$ Timing Diagram**
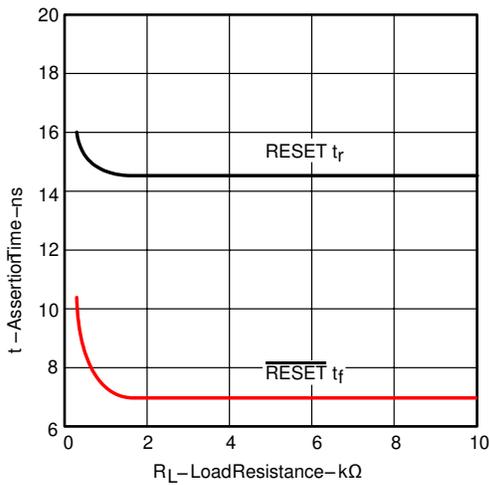
6.8 Typical Characteristics
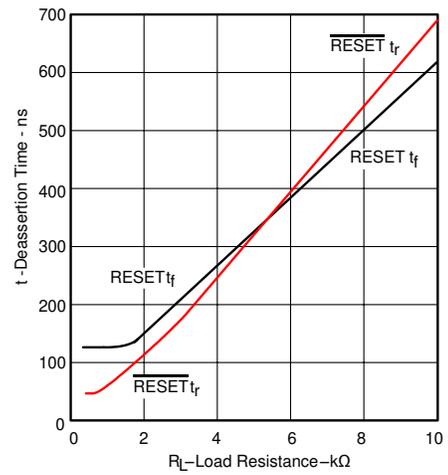

图 6-3. Assertion Time vs Load Resistance
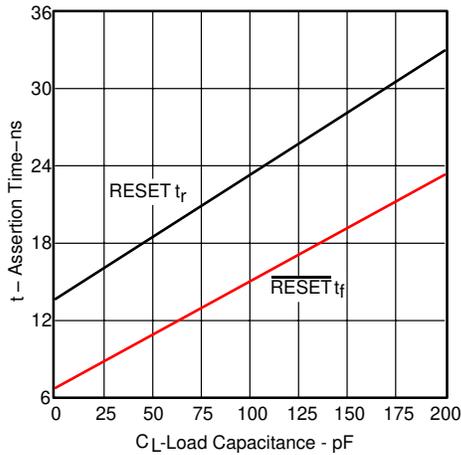
图 6-4. Deassertion Time vs Load Resistance

图 6-5. Assertion Time vs Load Capacitance
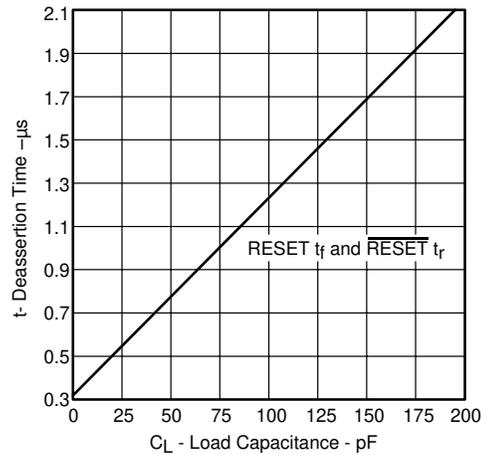
图 6-6. Deassertion Time vs Load Capacitance

7 Parameter Measurement Information
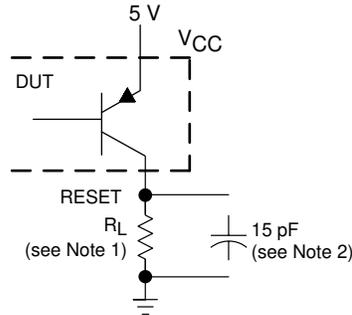
RESET OUTPUT CONFIGURATION

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A.   For I_{OL} and I_{OH}, R_L = 10 kΩ. For all switching characteristics, R_L = 511 Ω.

B.   This figure includes jig and probe capacitance.

图 7-1. RESET Output Configuration
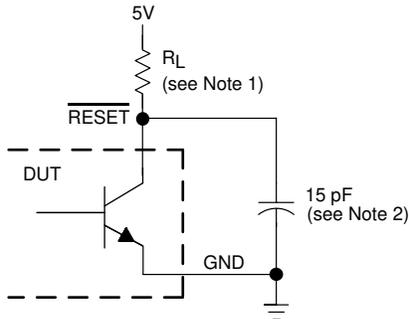
$\overline{\text{RESET}}$ OUTPUT CONFIGURATION

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A.   For I_{OL} and I_{OH}, R_L = 10 kΩ. For all switching characteristics, R_L = 511 Ω.

B.   This figure includes jig and probe capacitance.

图 7-2. $\overline{\text{RESET}}$ Output Configuration

图 7-3. Input Pulse Definition RESIN
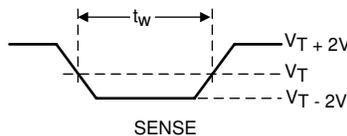
图 7-4. Input Pulse Definition SENSE

8 Detailed Description

8.1 Overview

The TL7702B, TL7705B, and TL7733B are integrated-circuit supply-voltage supervisors designed for use as reset controllers in microcomputer and microprocessor systems. The supply-voltage supervisor monitors the supply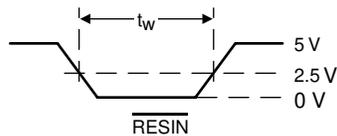 for undervoltage conditions at the SENSE input. During power up, the $\overline{\text{RESET}}$ output becomes active (low) when V_{CC} attains a value approaching 1 V. As V_{CC} approaches 3 V (assuming that SENSE is above V_{T+}), the delay-timer function activates a time delay, after which outputs $\overline{\text{RESET}}$ and RESET go inactive (high and low, respectively). When an undervoltage condition occurs during normal operation, outputs $\overline{\text{RESET}}$ and RESET go active. To ensure that a complete reset occurs, the reset outputs remain active for a time delay after the voltage at the SENSE input exceeds the positive-going threshold value. The time delay is determined by the value of the external capacitor C_T : $t_d \approx 2.6 \times 10^4 \times C_T$, where C_T is in farads (F) and t_d is in seconds (s).

An external capacitor (typically 0.1 µF) must be connected to REF to reduce the influence of fast transients in the supply voltage.

8.2 Functional Block Diagram

The functional block diagram is shown for illustrative purposes only; the actual circuit includes a trimming network to adjust the reference voltage and sense-comparator trip point.
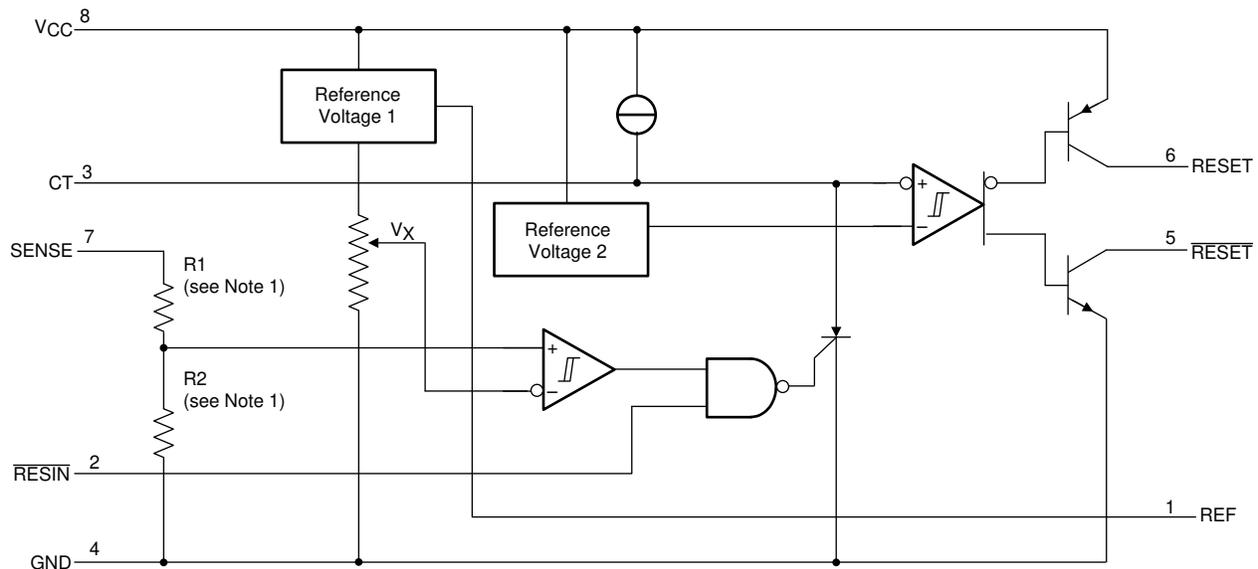
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8.3 Feature Description

8.3.1 Wide Supply-Voltage Range

The TL77xxB family operates using a wide supply voltage from 3.6 V to 18 V.

8.3.2 Adjustable Pulse Duration

The CT pin enables the ability to set a user-defined time delay in order to ensure that the fault condition is recognized. The external capacitor charges based on an internal current source until the voltage at the CT pin exceeds that of the internal reference voltage.

The time delay is determined by the value of the external capacitor C_T : $t_d \approx 2.6 \times 10^4 \times C_T$, where C_T is in farads (F) and t_d is in seconds (s).

The current source to charge the timing capacitor varies ±15%. Reference Voltage 2 is approximately 1.8 V and varies approximately ±5%. Once the timing capacitor charges, it discharges to about 0.6 V, not completely to 0 V.

8.4 Device Functional Modes

图 8-1 displays how the RESET and $\overline{\text{RESET}}$ output pins respond to the change in the the SENSE and $\overline{\text{RESIN}}$ input pins. When the $\overline{\text{RESIN}}$ pin is high, the RESET outputs are able to respond to a drop in the supply voltage at the SENSE pin. When the RESIN pin is low, the RESET and $\overline{\text{RESET}}$ pins are set HIGH and LOW respectively.
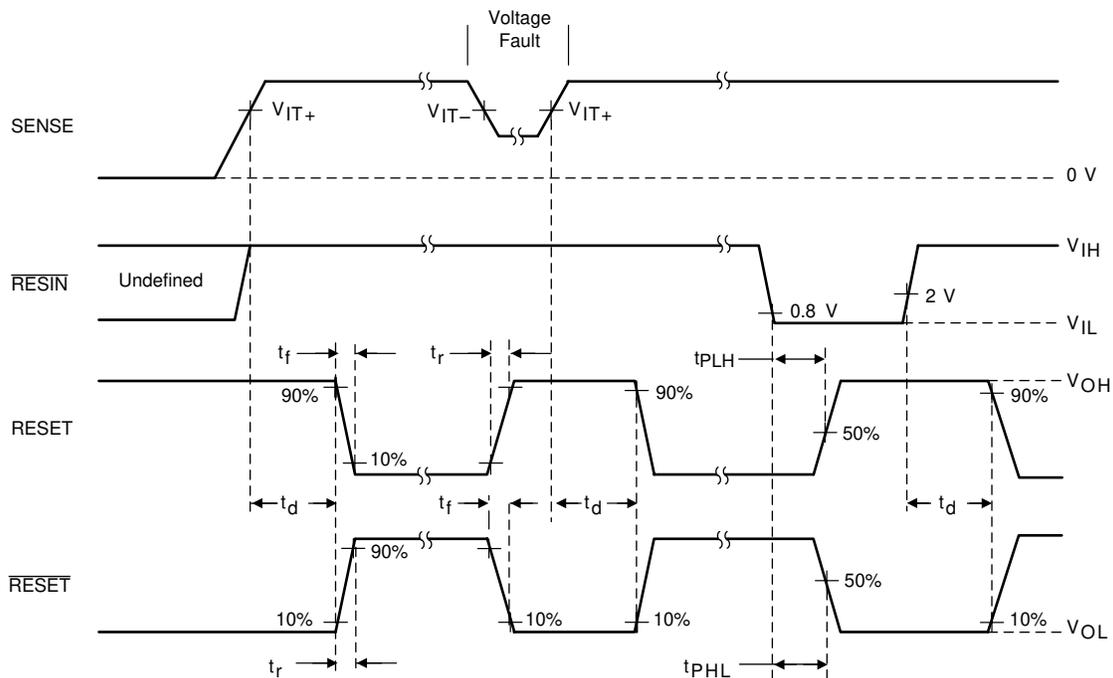
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图 **8-1. TL77xxB RESET and $\overline{\text{RESET}}$ Response and Timing**

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

图 9-1 shows an application where the TL7705B device is being used to sense the voltage supply for a microcontroller that is supplied with 5 V. If the voltage supply drops below the threshold voltage, the $\overline{\text{RESET}}$ pin is pulled LOW, signaling the microcontroller to reset.

9.2 Typical Application
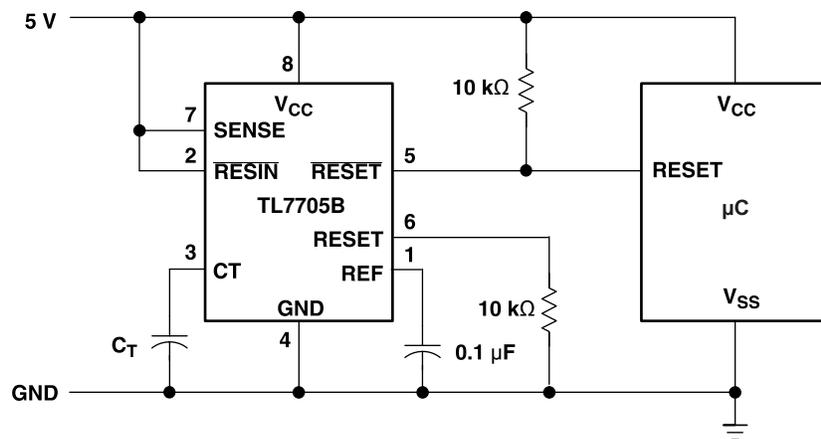
Copyright © 2016, Texas Instruments Incorporated

图 9-1. Reset Controller Schematic for a Microprocessor

9.2.1 Design Requirements

The external components required include the decoupling capacitor for the REF pin and the timing capacitor for the CT pin. Additionally, because the $\overline{\text{RESET}}$ output is open collector, a pullup resistor is required to ensure the correct HIGH level for the microcontroller RESET pin.

9.2.2 Detailed Design Procedure

TI recommends pullup and pulldown resistors of 10 kΩ.

To achieve a 2.6 ms time delay, use C_T = 0.1 µF.

Both outputs of the TL770xB must be terminated with similar value resistors, even when only one is being used. This prevents unwanted plateauing in either output waveform during switching, which may be interpreted as an undefined state or delay system reset

9.2.3 Application Curve
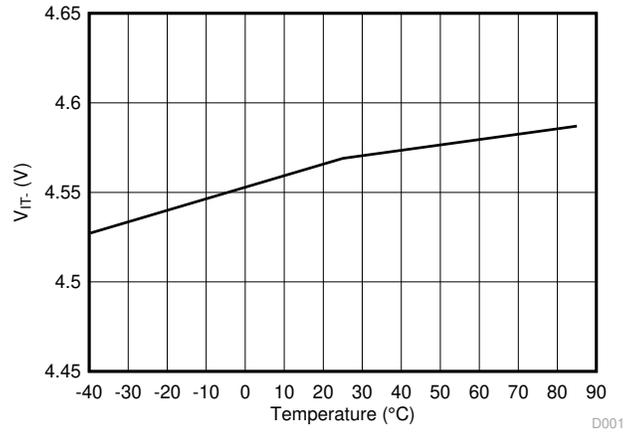
图 **9-2. TL7705B Threshold Voltage vs Temperature**

10 Power Supply Recommendations
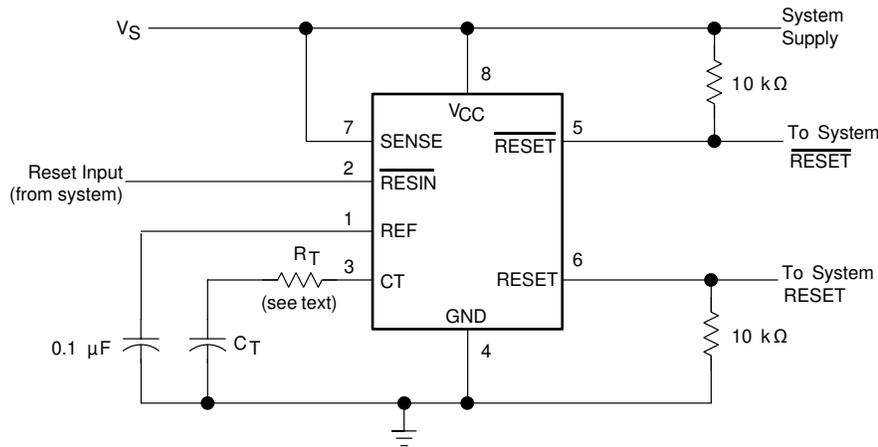
Copyright © 2016, Texas Instruments Incorporated

图 10-1. System Reset Controller With Undervoltage Sensing

When the TL770xB SENSE terminal is used to monitor V_{CC}, TI recommends a current-limiting resistor in series with C_T. During normal operation, the timing capacitor is charged by the onboard current source to approximately V_{CC} or an internal voltage clamp ($\approx$7.1-V Zener), whichever is less. When the circuit then is subjected to an undervoltage condition during which V_{CC} is rapidly slewed down, the voltage on CT exceeds that on V_{CC}. This forward biases a secondary path internally, which falsely activates the outputs. A fault is indicated when V_{CC} drops below $V_{(CT)}$, not when V_{SENSE} falls below V_{T-}.

Adding the external resistor, R_T, prevents false triggering. Its value is calculated as follows:

$$(V_{(CT)} - V_{T-}) / R_T \tag{1}$$

where

- $V_{(CT)}$ = V_{CC} or 7.1 V, whichever is less
- V_{T-} = 4.55 V (nom)
- R_T = value of series resistor required

For V_{CC} = 5 V

$$(5 - 4.55) / R_T < 1 \text{ mA} \tag{2}$$

Therefore,

$$R_T > 450 \ \Omega \tag{3}$$

Using a 20%-tolerance resistor, R_T should be greater than 560 Ω.

Adding this series resistor changes the duration of the reset pulse by no more than 10%. R_T extends the discharge of C_T, but also skews the $V_{(CT)}$ threshold. These effects tend to cancel one another. The precise percentage change can be derived theoretically, but the equation is complicated by this interaction and is dependent upon the duration of the supply-voltage fault condition.

Both outputs of the TL770xB must be terminated with similar value resistors, even when only one is being used. This prevents unwanted plateauing in either output waveform during switching, which may be interpreted as an undefined state or delay system reset.

11 Layout

11.1 Layout Guidelines

图 11-1 shows an example layout for the TL7705B device. As the $\overline{\text{RESET}}$ and RESET pins are open collector outputs, place pullup and pulldown resistors on the $\overline{\text{RESET}}$ and RESET pins respectively. A capacitor must be placed on the REF pin to stabilize the reference. This can help to prevent false triggering if noise couples into the reference.

11.2 Layout Example
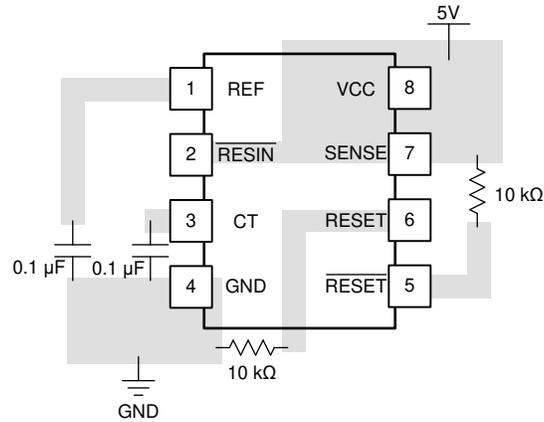
图 11-1. TL7705B Layout Example

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 12-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TL7702B	Click here	Click here	Click here	Click here	Click here
TL7705B	Click here	Click here	Click here	Click here	Click here
TL7733B	Click here	Click here	Click here	Click here	Click here

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者"按原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 术语表

TI 术语表   本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL7702BCD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7702BC	Samples
TL7702BCDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7702BC	Samples
TL7702BCDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7702BC	Samples
TL7702BCDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7702BC	Samples
TL7702BCP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL7702BCP	Samples
TL7702BCPE4	ACTIVE	PDIP	P	8	50	TBD	Call TI	Call TI	0 to 70		Samples
TL7702BID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7702BI	Samples
TL7702BIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7702BI	Samples
TL7702BIP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL7702BIP	Samples
TL7705BCD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	7705BC	Samples
TL7705BCDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	7705BC	Samples
TL7705BCDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	7705BC	Samples
TL7705BCDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	7705BC	Samples
TL7705BCP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL7705BCP	Samples
TL7705BID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	7705BI	Samples
TL7705BIDE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	7705BI	Samples
TL7705BIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	7705BI	Samples
TL7705BIP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL7705BIP	Samples
TL7705BQD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7705BQ	Samples
TL7705BQDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7705BQ	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL7705BQDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7705BQ	Samples
TL7705BQDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7705BQ	Samples
TL7733BCD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7733BC	Samples
TL7733BCDE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7733BC	Samples
TL7733BCDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7733BC	Samples
TL7733BCDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7733BC	Samples
TL7733BCDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7733BC	Samples
TL7733BCP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL7733BCP	Samples
TL7733BID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7733BI	Samples
TL7733BIDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7733BI	Samples
TL7733BIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7733BI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
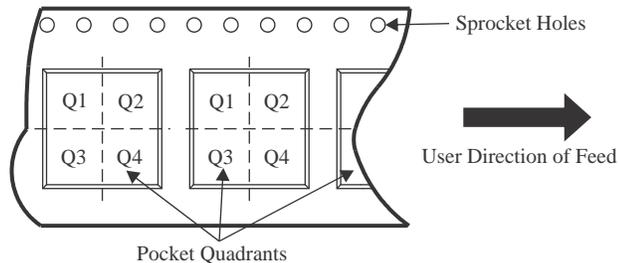
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL7702BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7702BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7705BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7705BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7705BQDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7705BQDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7733BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7733BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL7702BCDR	SOIC	D	8	2500	340.5	336.1	25.0
TL7702BIDR	SOIC	D	8	2500	340.5	336.1	25.0
TL7705BCDR	SOIC	D	8	2500	340.5	336.1	25.0
TL7705BIDR	SOIC	D	8	2500	340.5	336.1	25.0
TL7705BQDR	SOIC	D	8	2500	350.0	350.0	43.0
TL7705BQDRG4	SOIC	D	8	2500	350.0	350.0	43.0
TL7733BCDR	SOIC	D	8	2500	340.5	336.1	25.0
TL7733BIDR	SOIC	D	8	2500	340.5	336.1	25.0

![Texas Instruments logo]

PACKAGE MATERIALS INFORMATION

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width
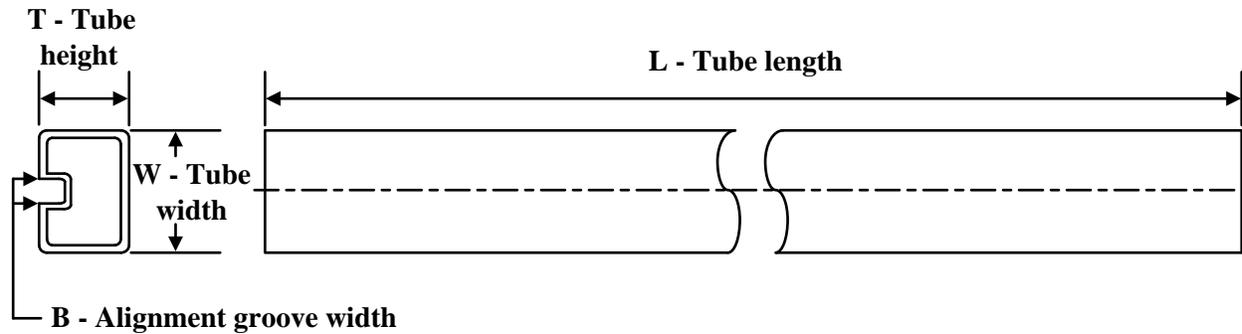
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL7702BCD	D	SOIC	8	75	507	8	3940	4.32
TL7702BCP	P	PDIP	8	50	506	13.97	11230	4.32
TL7702BID	D	SOIC	8	75	507	8	3940	4.32
TL7702BIP	P	PDIP	8	50	506	13.97	11230	4.32
TL7705BCD	D	SOIC	8	75	507	8	3940	4.32
TL7705BCP	P	PDIP	8	50	506	13.97	11230	4.32
TL7705BID	D	SOIC	8	75	507	8	3940	4.32
TL7705BIDE4	D	SOIC	8	75	507	8	3940	4.32
TL7705BIP	P	PDIP	8	50	506	13.97	11230	4.32
TL7705BQD	D	SOIC	8	75	505.46	6.76	3810	4
TL7705BQDG4	D	SOIC	8	75	505.46	6.76	3810	4
TL7733BCD	D	SOIC	8	75	507	8	3940	4.32
TL7733BCDE4	D	SOIC	8	75	507	8	3940	4.32
TL7733BCDG4	D	SOIC	8	75	507	8	3940	4.32
TL7733BCP	P	PDIP	8	50	506	13.97	11230	4.32
TL7733BID	D	SOIC	8	75	507	8	3940	4.32
TL7733BIDG4	D	SOIC	8	75	507	8	3940	4.32

.228-.244 TYP
[5.80-6.19]

PIN 1 ID AREA

A

1

8

6X .050
[1.27]

2X
.150
[3.81]

.189-.197
[4.81-5.00]
NOTE 3

4

5

B

.150-.157
[3.81-3.98]
NOTE 4

8X .012-.020
[0.31-0.51]

.010 [0.25] Ⓜ C A B

C

SEATING PLANE

.004 [0.1] C

4X (0°-15°)

.069 MAX
[1.75]

SEE DETAIL A

4X (0°-15°)

.005-.010 TYP
[0.13-0.25]

.010
[0.25]

0°- 8°

.016-.050
[0.41-1.27]

(.041)
[1.04]

.004-.010
[0.11-0.25]

DETAIL A
TYPICAL

4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

8X (.061)
[1.55]

SYMM
₵

SEE
DETAILS

1

8

8X (.024)
[0.6]

SYMM
₵

(R.002) TYP
[0.05]

4

5

6X (.050)
[1.27]

(.213)
[5.4]

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

METAL

SOLDER MASK
OPENING

SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK

EXPOSED
METAL

EXPOSED
METAL

.0028 MAX
[0.07]
ALL AROUND

.0028 MIN
[0.07]
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED
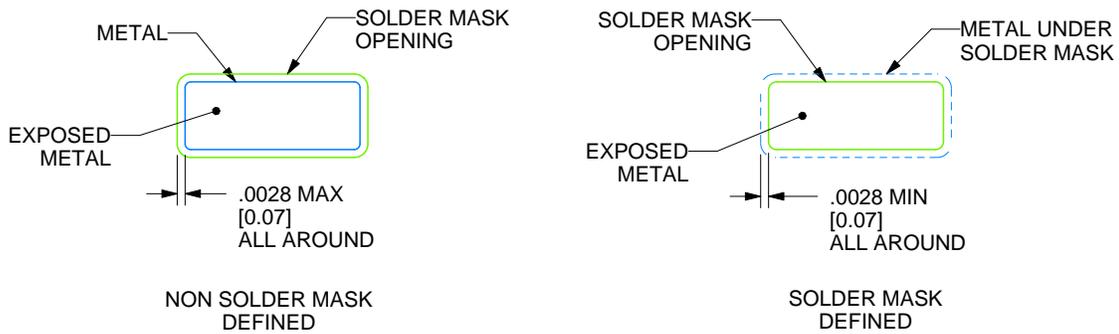
SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)
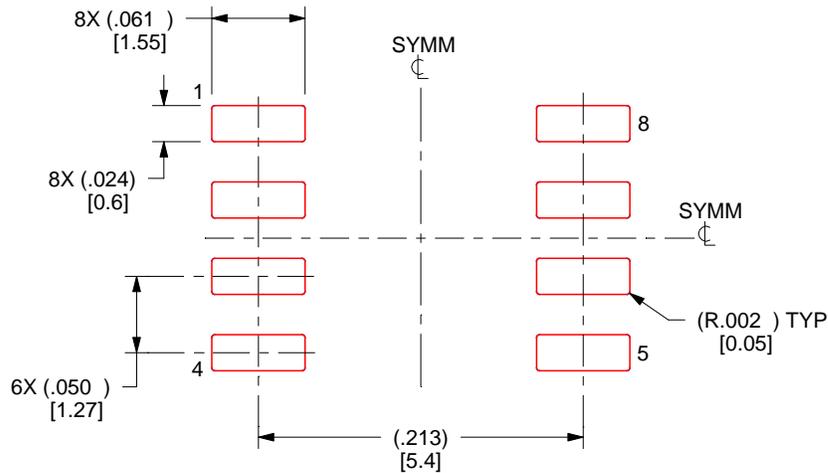
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

8X (.061)
[1.55]

1

8X (.024)
[0.6]

6X (.050)
[1.27]

4

SYMM
℄

SYMM
℄

8

5

(R.002) TYP
[0.05]

(.213)
[5.4]

SOLDER PASTE EXAMPLE
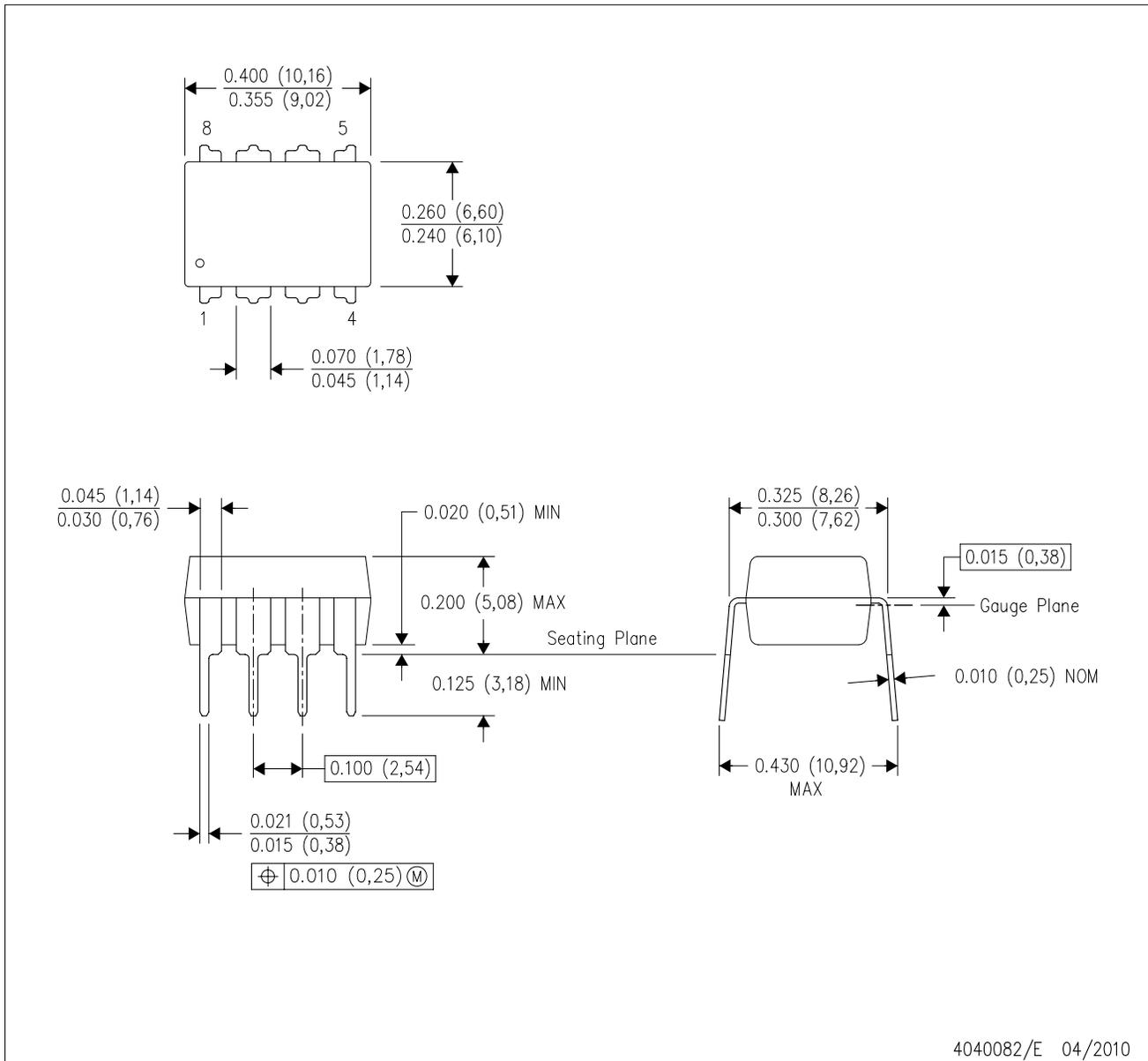BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C   02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R—PDIP—T8)   PLASTIC DUAL—IN—LINE PACKAGE

0.400 (10,16)
0.355 (9,02)

8   5

0.260 (6,60)
0.240 (6,10)

1   4

0.070 (1,78)
0.045 (1,14)

0.045 (1,14)
0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92)
MAX

4040082/E 04/2010

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Falls within JEDEC MS—001 variation BA.

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